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Fault tolerant reconfigurable shift register architecture using CNTFET

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ABSTRACT

Advance in the technology has made the development in the nano devices. Which plays a vital role in the area, low power and reduced delay. In this paper a reconfigurable shift register architecture has been designed using RR-Gate. This architecture is implemented in both MOSFET (metal–oxide–semiconductor field-effect transistor) and CNTFET (carbon nanotube field-effect transistor) technology. This architecture dissipates low power as its implementation has been carryout using the fault tolerant reversible logic so the occurrence of the error is very much limited.

Keywords: Reversible Logic, Fault tolerant, reconfigurable architecture, RR-Gate.

INTRODUCTION

According to Gordon Moore, shrinking the dimensions will make the device to operate at the higher speed for the same power per unit area. As increasing package and shrinking of device leads to increase of tunnelling current and short channel effect lets to the invention of new device with the change in the channel material (CNTFET).Carbon nanotube FETs (CNTFETs) offer high-performance electronic devices due to the advantages such as a high electron velocity, a high current driving capability and an energy band structure with direct transition (Rosenblattet, 2005). Physical reversibility can provide all the advantage of the reversibility. No heat dissipation will take place when the device is employed with physical reversibility. As all the fault tolerant gates are reversible gates which Satisfy the reversible logic along with the parity preserving fault tolerant property (Javey, 2004). Detection and correction of errors is so convenient when the components of system are fault tolerant. In communication and many other systems fault tolerance can be achieved by employing same parity on the input and output. Therefore, the development of nanotechnology, fault tolerant reversible systems and parity preserving reversible circuits will be the most popular designs in the future.

MATERIALS AND METHODS

Fault tolerant Reversible Logic: The fault tolerant devices are required as the testing cost is too high and the devices are not reusable or error diagnosis and correction too difficult. 1) Reversible circuits have an equal number of inputs and outputs. 2) Fanout is not allowed. 3) Every output of a gate that is not used in the circuit is a garbage signal. A good synthesis method minimizes the number of garbage signals. 4) The total number of constants at inputs of the gates should be kept as low as possible (Parhami, 2006). These makes the traditional methods inapplicable. Fault tolerant nature in reversible logic can be obtained by one to one mapping and it can be readily checked by xor the inputs and will be equal to the xor of the outputs.

Reconfigurable shift register architecture: Reconfigurable architecture is an architecture which can able to perform all the four types of shift register operation like SISO, SIPO, PISO, PIPO depending on the selection lines s0 and s1. When the selection line s0=0 and s1=0 then it perform the operation of PISO. When the selection line s0=0 and s1=1 then it perform the operation of SISO. When the selection line s0=1 and s1=0 then it perform the operation of SIPO. When the selection line s0=1 and s1=1 then it perform the operation of PIPO. This structure is designed using RR-Gate (S.Ranjith.et.al,2013)dissipates less power than the existing structures as it has used the reversible and fault tolerant logic gates for the design. This structure can be used where there is necessity of different shift registers in different time using the selection signal we can control the performance of this architecture.

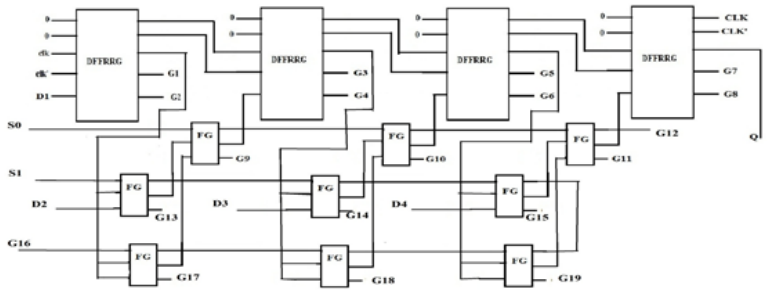

Fig.1. Reconfigurable shift register architecture using RR- Fault Tolerant Reversible Logic Gate.

CNTFET: Carbon Nano Tube Field Effect Transistor (CNTFET) is the alternating device for the MOSFET which has been in existence. As moving to the nano level the MOSFET dissipates leakage power much to overcome this an alternative device called CNTFET has been still in Research level. Here in this paper we have used 32nm CNTFET to design this RR-gate and using which the reconfigurable architecture in Fig.1 has been illustrated (S.Ranjith, 2014).

RESULTS & DISCUSSION

This reconfigurable architecture has been simulated using Synopsis Tool and the Power Dissipation comparison in Table.1 has been made for the implementation using 130nm MOSFET, 32nm MOSFET, 32nm CNTFET. RA-Reconfigurable architecture working in all four shift register models. This architecture has been made to operate as SISO, SIPO, PISO, PIPO individually and also combined form and their corresponding power dissipation has been illustrated in the table1.

Table.1. Power dissipation comparison of Reconfigurable Architecture in different technology.

Technology	SISO	PIPO	PISO	SIPO	RA
130 MOSFET	1.273E-03	1.133E-03	8.105E-04	1.273E-03	1.133E-03
32 MOSFET	1.916E-04	1.984E-04	2.012E-04	1.926E-04	1.960E-04
32 CNTFET	1.625E-05	7.297E-05	1.149E-05	1.625E-05	7.341E-05

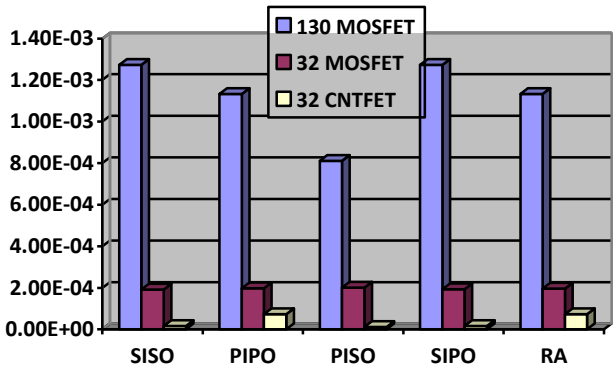

Chart.1. Power dissipation comparison of Reconfigurable Architecture in different technology.

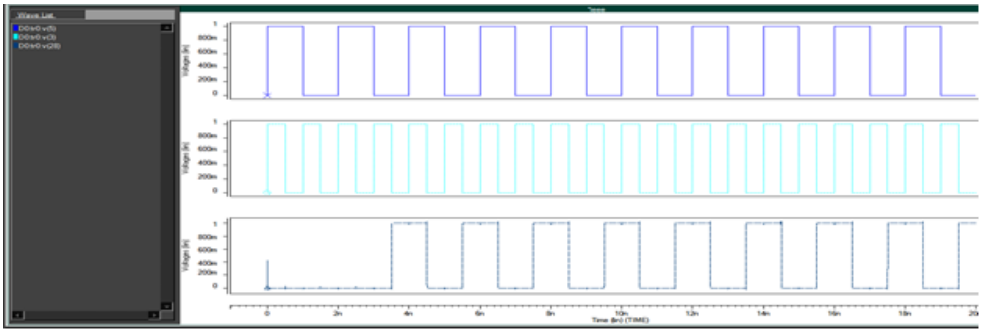

Fig.2. Reconfigurable architecture operating as SISO

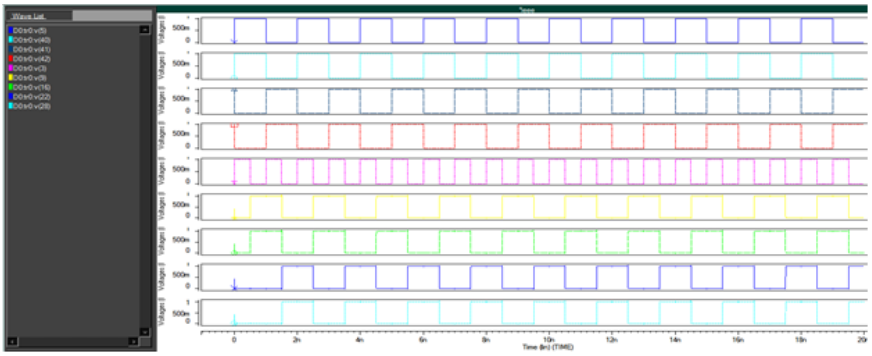

Fig.3. Reconfigurable architecture operating as PIPO

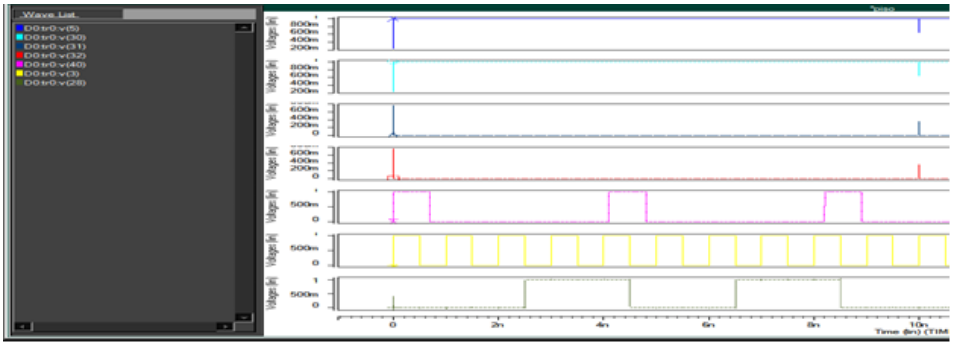

Fig.4.Reconfigurable architecture operating as PISO

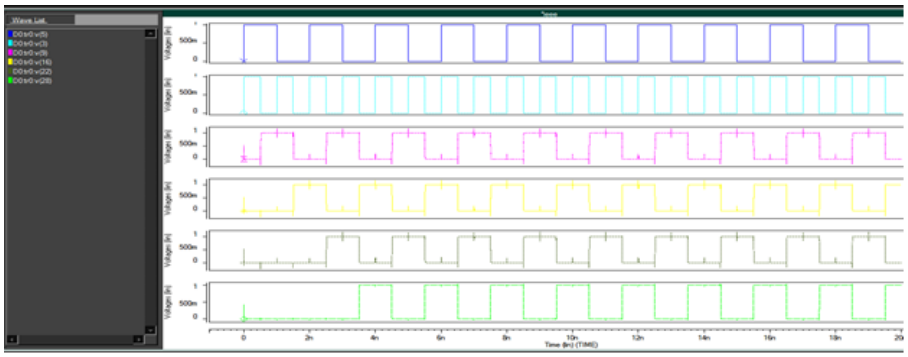

Fig.5. Reconfigurable architecture operating as SIPO

CONCLUSION

The work say illustrates the reconfigurable shift registers architectures which has been designed using RRfaulttolerant reversible logic gate which is less prone to error of faults and identification of fault is also simple. These designs are carried out using the MOSFET and CNTFET technologies and simulated and power analysis has been done using Synopsis Hspice tool using 130nm MOSFET, 32nm MOSFET, 32nm CNTFET.

REFERENCES

Javey, A., Guo, J., Farmer, D. B., Wang, Q., Yenilmez, E., Gordon, R. G., Lundstrom, M., and Dai, H. 2004 Nano Lett.7, 1319 (2004).

Parhami, Fault tolerant reversible circuits, in Proceedings of 40th Asimolar Conf. Signals, Systems, and Computers, Pacific Grove, CA, 1726-1729, 2006.

Rosenblattet, S. et al., Appl. Phys. Lett. 87, 153111 (2005).

S.Ranjith, An Approach for the Reduction of Leakage Power Using Low Power Technique, International Journal of Applied Engineering Research, 9(25), 2014, 8670-8681

S.Ranjith, T.Ravi, E. Logashanmugam, Design and Analysis of Parity Preserving Fault Tolerant Reversible Logic Shift Registers Using New 4*4 RR-Gate, International Journal of Advanced Research in Computer Science and Electronics Engineering (IJARCSEE), 2(2), 2013

S.Ranjith, T.Ravi, P.Umarani, R.Arunya, Design of CNTFET Based Sequential Circuits Using Fault Tolerant Reversible Logic, International Journal of Applied Engineering Research, 9, 2014, 25789-25804

S.Ranjith, T.Ravi, V.Kannan, Design of Shift Registers Using Conservative Parity Preserving Fault Tolerant Fredkin gate, Proceedings of National Conference on Recent Trends in Modern Electronics and its Applications, 2013, 7-8

S.Ranjith, T.Ravi, V.Kannan, Fault Tolerant Reversible Logic D-Flip Flop Based Shift Registers In 32nm CMOS Technology, International Journal of Engineering Research & Technology (IJERT), 2(2), 2013

T.Ravi, S.Ranjith, V.Kannan, A Novel Design of D-Flip Flop Using New RR Fault Tolerant Reversible Logic Gate, International Journal of Emerging Technology and Advanced Engineering, 3(2), 2013.